

# KF351

## Single Operational Amplifier (JFET)

#### **Features**

• Internally trimmed offset voltage: 10mV

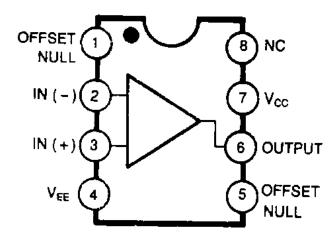
Low input bias current: 50pA
Wide gain bandwidth: 4MHz
High slew rate: 13V/μs
High input impedance: 10<sup>12</sup>Ω

### **Description**

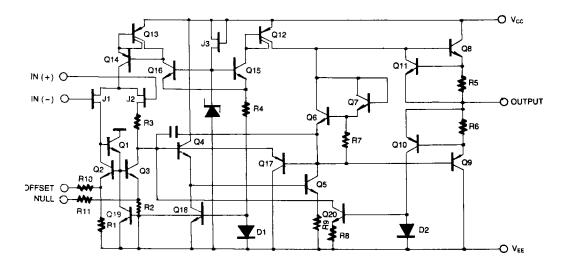
The KF351 is JFET input operational amplifier with an internally compensated input offset voltage. The JFET input device provides wide bandwidth, low input bias currents and offset currents.



### **Internal Block Diagram**



## **Schematic Diagram**



## **Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit	
Supply Voltage	Vcc	±18	V	
Differential Input Voltage	V <sub>I</sub> (DIFF)	30	V	
Input Voltage Range	VI	±15	V	
Output Short Circuit Duration	-	Continuous	-	
Power Dissipation	PD	500	mW	
Operating Temperature	TOPR	0 ~ +70	-70 °C	
Storage Temperature Range	TSTG	-65 ~ +150	°C	

### **Electrical Characteristics**

(VCC = + 15V, VEE = - 15V, TA = 25  $^{\circ}$ C. unless otherwise specified)

Parameter	Symbol	Con	nditions	Min.	Тур.	Max.	Unit
Input Offset Voltage	Vio	$R_S = 10k\Omega$		-	5.0	10	mV
			0 °C≤T <sub>A</sub> ≤70 °C	-	-	13	IIIV
Input Offset Voltage Drift (Note1)	ΔV10/ΔΤ	$R_S = 10k\Omega$	0 °C≤T <sub>A</sub> ≤70 °C	-	10	-	μV/°C
Input Offset Current	lio			-	25	100	pА
			0 °C≤T <sub>A</sub> ≤70 °C	-	-	4	nA
Input Bias Current	IBAIS			-	50	200	pА
			0 °C≤T <sub>A</sub> ≤70 °C	-	-	8	nA
Input Resistance (Note1)	Rı		-	-	10 <sup>12</sup>	-	Ω
Large Signal Voltage Gain	GV	VO(P-P)= ± 1	10V	25	100	-	V/mV
		R <sub>L</sub> =2kΩ	0 °C≤T <sub>A</sub> ≤70 °C	15	-	-	] "/!!!
Output Voltage Swing	VO(P-P)	$R_L = 10k\Omega$		±12	±13.5	-	V
Input Voltage Range	V <sub>I(R)</sub>		-	±11	+15 -12	-	V
Common Mode Rejection Ratio	CMRR	Rs ≤ 10kΩ		70	100	-	dB
Power Supply Rejection Ratio	PSRR	Rs≤10kΩ		70	100	-	dB
Power Supply Current	Icc		-	-	2.3	3.4	mA
Slew Rate (Note1)	SR	G∨ = 1		-	13	-	V/µs
Gain-Bandwidth Product (Note1)	GBW			ı	4	-	MHz

#### Note:

1. Guaranteed by design.

### **Mechanical Dimensions**

### **Package**

### **Dimensions in millimeters**

## 8-DIP 0.79 6.40 ±0.20 0.252 ±0.008 $1.524 \pm 0.10$ 0.060 ±0.004 0.46 ±0.10 $0.018 \pm 0.004$ #8 9.20 ±0.20 0.362 ±0.008 $\frac{9.60}{0.378}$ MAX #5 2.54 $\frac{5.08}{0.200}$ MAX 3.30 ±0.30 0.130 ±0.012 7.62 0.300 $\frac{0.33}{0.013}\,\text{MIN}$ $3.40 \pm 0.20$ $\overline{0.134 \pm 0.008}$ $0.25^{\,+0.10}_{\,\,-0.05}\atop -0.010^{\,+0.004}_{\,\,-0.002}$ \_0~15°

## **Ordering Information**

Product Number	Package	Operating Temperature
KF351	8-DIP	0 ~ + 70°C

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com